Differential VCO and Frequency Tripler using SiGe HBTs for the 24 GHz ISM Band

Mina Danesh[1], Frank Gruson[2], Peter Abele[2], and Hermann Schumacher[2]

[1]Harris Corporation, Microwave Communications Division, Montreal, QC, H9B 3G4, Canada
[2]University of Ulm, Dept. of Electron Devices and Circuits, 89069 Ulm, Germany

Abstract — **A frequency source generator chip was designed and built in a commercial SiGe process for an integrated front-end transceiver operating in the 24 GHz ISM band. It consists of a negative resistance cross-coupled differential VCO, oscillating at 8 GHz with a 150 MHz tuning range, having an output power of 0 dBm and a phase noise of -90 dBc/Hz at 100 kHz offset. The VCO drives a differential amplifier used as a frequency tripler which results in an overall voltage control frequency source operating at a nominal frequency of 23.5 GHz with a 420 MHz tuning range. It has a -10 dBm output power and consumes 180 mW. Its phase noise is –80 dBc/Hz at 100 kHz. The total chip area measures 600 x 300 μm².**

I. Introduction

Short-range wireless data link and short-range automotive radar sensors operating in the 24 – 24.25 GHz ISM band require fully integrated, low-cost RF front-end ICs. While until recently MMICs based on GaAs technology have been used, advances in SiGe-HBT technology allow for the realization of these circuits using low-cost silicon-based technology.

This paper presents a 24 GHz source based on an 8 GHz VCO driving a frequency tripler. This building block is to drive the LO port of a Gilbert cell mixer which is the heart of many transceivers. The purpose is to investigate this configuration instead of a 24 GHz VCO [1]-[3], and moreover, its advantage gives an easier integration with lower frequency circuitry, such as the frequency divider used in the PLL synthesizer.

The MMIC is fabricated using Atmel's SiGe1 HBT process which features standard HBTs (f_T = 30 GHz) with high breakdown voltages, and high speed HBTs with selectively implanted collector (f_T = 50 GHz) with BV_{ceo} = 3.5 V. With this process, 2 metal (Al) layers are used.

The purpose of using differential circuits resides in a better integration with the frequency tripler topology, the differential-type frequency divider, and the Gilbert-type mixer. Differential circuits have better common-mode rejection, twice the maximum voltage swing at a given supply voltage, and reduced crosstalk, however, at the expense of higher noise due to a double count of transistors, larger chip area, and power consumption. Moreover, only differential VCOs are suited for integration on lossy silicon substrates together with other building blocks, in order to minimize substrate crosstalk.

II. Circuit Design

A. Voltage Controlled Oscillator

The circuit design of the VCO is based on a cross-coupled differential pair, realized as a negative resistance oscillator, as shown in Fig. 1. The differential design allows for twice the output swing compared with a single-ended oscillator and does not create AC voltage drops across the supply lines. It also simplifies the integration with other building blocks.

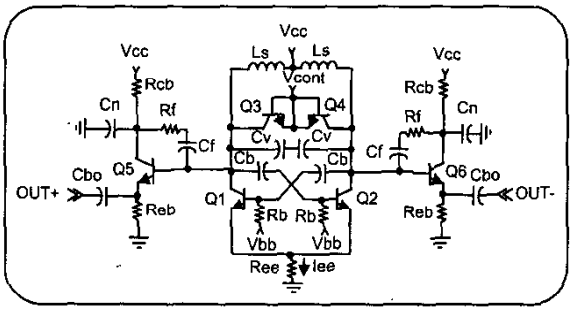

Fig. 1. Differential VCO and buffer schematic.

The LC tank consists of Ls, Cv, and Q3/Q4 used as varactors, but due to the presence of Cb in the feedback path, its influence must also be taken into account. Cb provides regenerative feedback from the output to the base of Q1/Q2, allowing for a higher output voltage swing. Transistors Q3 and Q4 have a reverse-biased base-emitter junction configuration. The low varactor quality-factor (Q) is limited by the intrinsic series resistance of the device. The combined varactor and Cv equivalent peak Q is 5.8 at 12 GHz. The tank inductor consists of a 3-turn square

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symmetric microstrip inductor, simulated as a 3-port element in an EM simulator [4]. An inductance Ls of around 0.4 nH has been chosen, such that a capacitance Cv of more than 0.1pF could be added to improve phase noise. Figure 2 shows the inductor which uses a single metal layer M2, on a 20 Ω-cm bulk Si resistivity substrate. It has a 2.2 Ω DC resistance, a differential Q of 10 at 8 GHz (see Fig. 3), and self-resonates beyond 20 GHz.

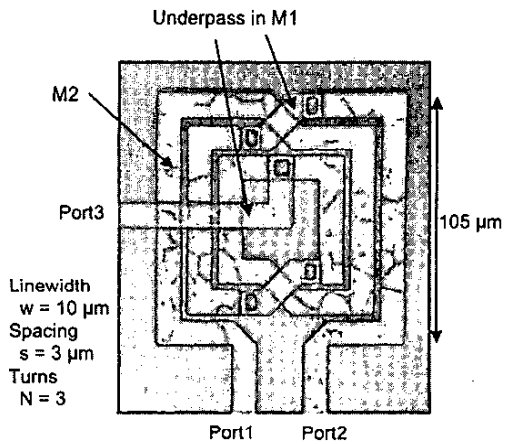

Fig. 2. Microphotograph of the VCO symmetric spiral inductor.

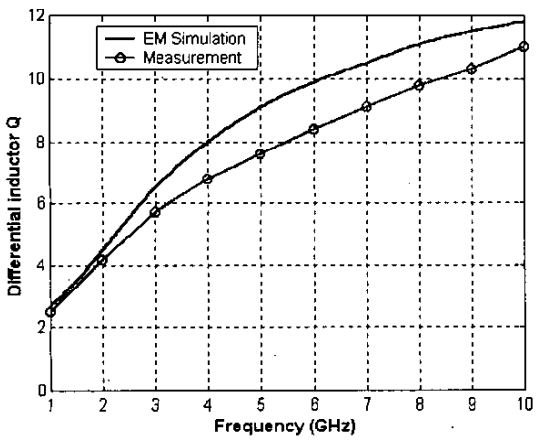

Fig. 3. Simulated and measured differential Q of the VCO inductor.

In order to provide minimal loading to the VCO tank, an emitter follower buffer amplifier at the output of the VCO was used. The follower provides impedance transformation to drive a 50 Ω load and avoids oscillator pulling. Due to the large resonator voltage at the output of the VCO, the buffer will operate as a limiter.

The VCO was simulated using MEXTRAM models for the HBTs, equivalent models for the MIM capacitors, and simulation data for the spiral inductor. The inductor layout was automatically generated using a custom script. The VCO was optimized for a 7.9 GHz output center frequency with a 200 MHz tuning range over 2.8 V, and a phase noise of -90 dBc/Hz at 100 kHz, suitable for FM or BPSK modulation. With a power consumption of 44 mW, the VCO gives 5 dBm differential output power.

B. Frequency Tripler

Frequency tripler FET multipliers are widely used in a single-ended topology designed with input and output matching networks [5], [6]. Conversion efficiencies of 10% at 38 GHz were obtained [7]. Instead, this paper presents a frequency tripler using SiGe HBTs as part of a differential transistor pair. The differential pair is driven with high input voltage swing (Vpp > 4kT/q=100mVpp), and therefore, acts as a limiting amplifier, ideally producing a square wave. In addition to the fundamental, this kind of amplifier produces odd number of harmonics since the differential topology permits the cancellation of the even harmonics. The load of the amplifier is tuned to the third harmonic in order to peak the third harmonic, therefore maximizing conversion gain of the tripler.

The tripler schematic is shown in Fig. 4. Passive components, Ls and Cs (0.12 pF), were chosen in order to have resonance at 24 GHz for output power optimization and good matching at the output. The symmetric inductor is designed for a 0.32 nH (Ls*2) total inductance. It has a differential Q of 13 at 24 GHz, and a self-resonance of greater than 40 GHz.

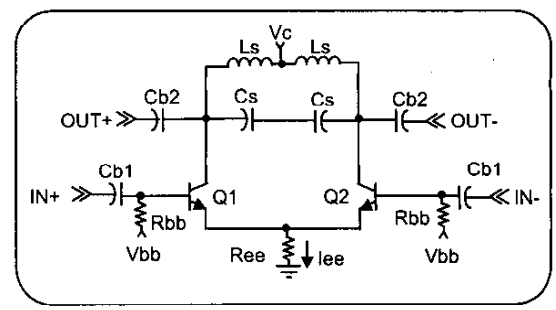

Fig. 4. Differential amplifier schematic used as the frequency tripler.

The frequency tripler was simulated and optimized for a differential output power of –4 dBm, for an input power of 5 dBm at 8 GHz, with a current consumption of 30 mA at 3.3 V. Therefore, the tripler has a 9 dB conversion loss and an RF-to-RF efficiency of 12.6%. The second harmonic rejection is -25 dBc. The phase noise degradation depends

on the multiplication factor. For a tripler, 9.5 dB is added to the VCO phase noise [7].

III. Implementation and Measurement Results

On-wafer measurements were performed to validate simulated results. Separate VCOs and frequency triplers were built and tested. In order to perform differential measurements, 3dB 180° hybrids with phase matched cables were used at the input and output ports.

A. VCO Results

Single VCO chips were built which validate simulated results. The VCO oscillates at 7.93 GHz with a 0 V control voltage. Figure 5 shows its measured frequency tuning range. A total of 270 MHz tuning range was achieved with a control voltage from –3 V to 2.7 V. The VCO has an output power of 4.4 dBm (+/- 0.1 dBm) through the frequency range. Its measured average phase noise from the spectrum analyzer is –90 dBc/Hz at 100 kHz.

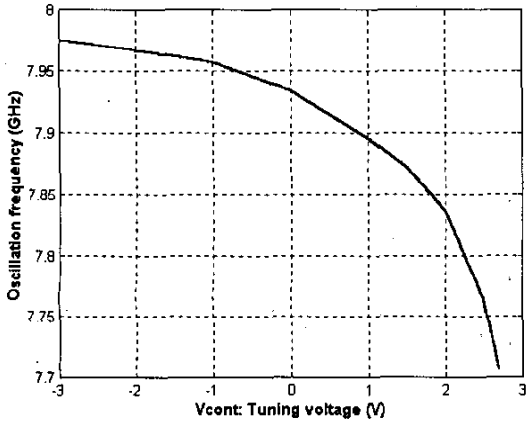

Fig. 5. Measured tuning range of the VCO with buffer.

B. Frequency Tripler Results

The tripler chip output signal was measured on the spectrum analyzer while injecting an 8 GHz signal from a signal generator. The maximum achievable output power is –8 dBm when the input power is greater than 0 dBm (see Fig. 6) for a current consumption of 28 mA at 3.3 V. The fundamental tone and the second harmonic have 7 dB and 15 dB rejection, respectively. It was also verified that the optimized output power was obtained with an input frequency of 8 GHz. The discrepancies between tripler measurements (higher loss and lower rejection) and simulations can be partly explained by inaccurate modeling of active and passive components at higher frequencies because of parasitics and limitations of the process, and as important, by the differential measurement equipment.

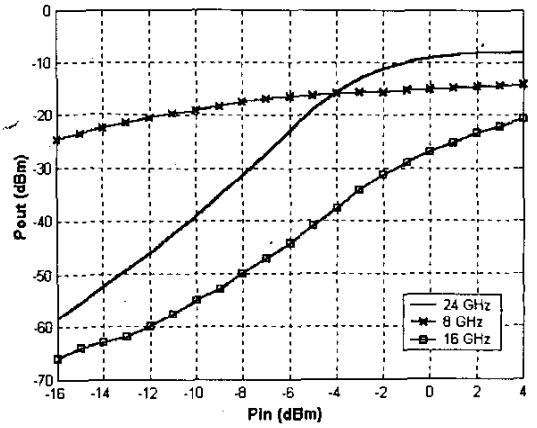

Fig. 6. Measurement of the frequency tripler output.

C. VCO / Tripler Results

The VCO and tripler were integrated into one circuit which was then re-optimized in order to adapt the VCO/buffer output to the tripler input, mainly by adjusting the biasing currents. Figure 7 shows the MMIC layout, which measures 600 x 300 μm^2.

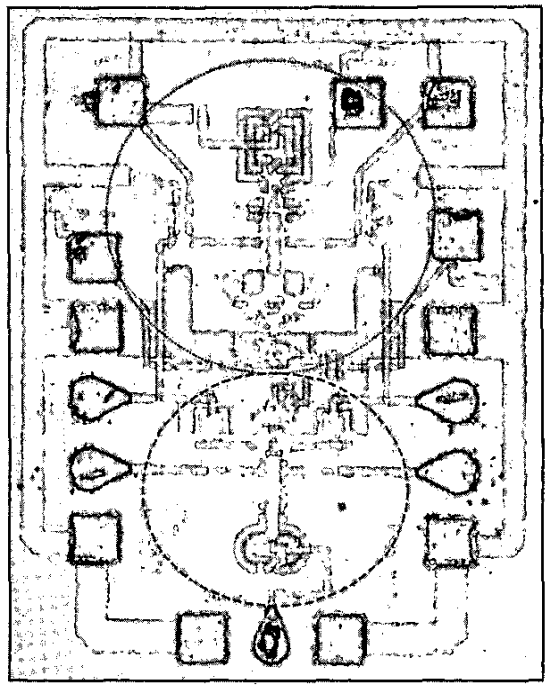

Fig. 7. Microphotograph of the VCO / tripler MMIC layout.

At the tripler output, both fundamental and third harmonic signal levels are at around –10 dBm, whereas the second harmonic has a 20 dB rejection (see Table I). Measured and simulated results agree well except for the lower tripler output power. A better output matching could be investigated. The added losses could be compensated by increasing the power consumption of the tripler only, to reach a 0 dBm output, enough to drive the mixer. The tripler and VCO frequency tuning ranges of 420 MHz and 144 MHz, respectively, were obtained over 2.5 V, as shown in Fig. 8. The VCO oscillates initially at 7.82 GHz (and up to 8.03 GHz for lower power versions when a 0 V control voltage is applied), and the average phase noise was measured to be –89 dBc/Hz at 100 kHz carrier offset. Therefore, the phase noise at 23.5 GHz is around –80 dBc/Hz at 100 kHz, achieving better VCO phase noise results than reported [1], [2]. The total current consumption is 55 mA at 3.3 V.

TABLE I
MEASURED DIFFERENTIAL OUTPUT POWER FOR THE VCO AND THE TRIPLER FROM THE VCO/TRIPLER MMIC.

Frequency (GHz)	VCO output (dBm)	Tripler output (dBm)
7.82 / *7.81*	**0.5** / *2.6*	**-9** / *-8.8*
15.6 / *15.6*	**-33** / *-32*	**-30** / *-37*
23.5 / *23.4*	**-34.5** / *-33*	**-10** / *-4*

Values in italic indicate simulated results.

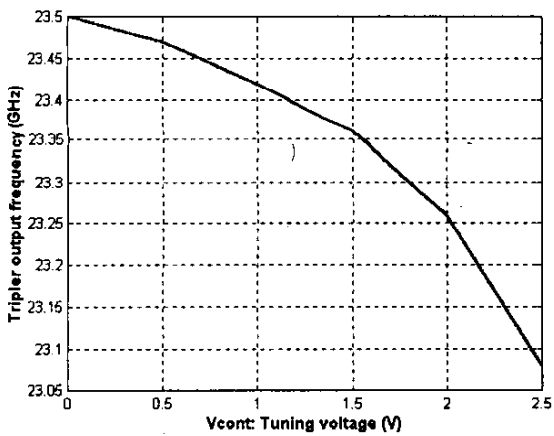

Fig. 8. Measured tripler output tuning range from the VCO / tripler MMIC.

IV. CONCLUSION

An integrated variable frequency source suitable for the 24 GHz ISM band was presented. The VCO followed by a frequency tripler were both differentially driven using SiGe HBTs and symmetric microstrip spiral inductors. This paper featured a novel frequency tripler circuit topology built in a SiGe process, whereas conventional designs were done in GaAs. An oscillation frequency of around 7.9 GHz was obtained at the output of the VCO, and the measured phase noise is -90 dBc/Hz at 100 kHz offset, over a 150-200 MHz tuning range. This signal is to be fed directly to a frequency divider in the PLL. The phase noise may be further enhanced by optimization of the inductor. Atmel's SiGe1 process now offers 3 metal layers with thicker metallization. The VCO/tripler frequency source MMIC results in a 23.5 GHz output frequency with a frequency tuning range of 420 MHz, a phase noise of –80 dBc/Hz at a 100 kHz offset, and an output power of –10 dBm, for a total power consumption of 180 mW. This paper demonstrated the feasibility of building 24 GHz low cost MMIC frequency sources in a commercial SiGe production process.

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